IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of )
)
SATO et al. )
)
Application Number: To be assigned )
)
Filed: Concurrently herewith )
)
For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR DESIGNING LOGIC INTEGRATED CIRCUIT )

D5/9
5-20-02

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Applicants have amended the claims in order to remove the multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment. Prior to an examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Please substitute claims 3 and 4 currently on file with the following amended claims.

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3. (Amended) A semiconductor integrated circuit according to claim 1, wherein the storing means are a volatile memory.

4. (Amended) A semiconductor integrated circuit according to claim 1, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read